METHOD AND APPARATUS FOR PROVIDING WELL-MATCHED SOURCE AND SINK CURRENTS

Background

[0001] Charge pumps of phase-locked loops (and other devices) require well-matched source and sink currents. Unfortunately, component manufacturing tolerances, signal noise and other factors can make obtaining well-matched source and sink currents difficult.

Summary of the Invention

[0002] One aspect of the invention is embodied in apparatus for providing well-matched source and sink currents. The apparatus comprises a number of parallel current paths, a first of which drives a first current mirror to mirror current to second and third of the parallel current paths. The second parallel current path provides well-matched source and sink currents as outputs. The third parallel current path is matched to the second. Fourth and fifth of the parallel current paths each comprise a transistor of a current steering mechanism and a bias transistor. A first transistor of the current

steering mechanism is coupled in the fourth current path and is driven by feedback from the third current path. A second transistor of the current steering mechanism is coupled in the fifth current path and is driven by a reference voltage. The bias transistor of the fourth current path mirrors current to the first current path under control of the current steering mechanism, and the bias transistor of the fifth current path mirrors current to the second and third current paths under control of the current steering mechanism. A second current mirror is driven by a bias current and mirrors the bias current to each of the number of parallel current paths.

[0003] Another aspect of the invention is embodied in a method for providing well-matched source and sink currents. The method comprises mirroring a bias current to each of a number of parallel current paths of a circuit. The bias current is then mirrored again, from a first of the parallel current paths to second and third of the parallel current paths (with the second and third current paths being matched). A reference voltage, and feedback from the circuit, is provided to a current steering mechanism comprising fourth and fifth of the parallel current paths. Current is then steered between the first and second current paths by means of the current steering mechanism. The well-matched source and sink currents are output from the second current path.

[0004] Other embodiments of the invention are also disclosed.

Bri f Description of the Drawings

[0005] Illustrative embodiments of the invention are illustrated in the drawings, in which:

[0006] FIG. 1 illustrates a first exemplary circuit for providing well-matched source and sink currents;

[0007] FIG. 2 illustrates a second exemplary circuit for providing well-matched source and sink currents;

[0008] FIG. 3 illustrates a third exemplary circuit for providing well-matched source and sink currents;

[0009] FIG. 4 illustrates an exemplary method for providing well-matched source and sink currents;

[0010] FIG. 5 illustrates a first prior art method for providing source and sink currents; and

[0011] FIG. 6 illustrates a second prior art method for providing source and sink currents.

Detailed Description of the Invention

[0012] FIG. 1 illustrates a first exemplary circuit 100 for providing well-matched source and sink currents. In general, the circuit 100 comprises a number of parallel current paths 102, 104, 106, 108, 110. A first of the parallel current paths 102 drives a first current mirror 112 to mirror current to second and third of the parallel current paths 104, 106. A second of the

parallel current paths 104 provides well-matched source and sink currents (I1, I2) as outputs. A third of the parallel current paths 106 is matched to the second 104. The third current path may be used to provide feedback in the circuit 100, as will be explained in the next paragraph.

[0013] Fourth and fifth of the parallel current paths 108, 110 each comprise a transistor of a current steering mechanism 114, as well as a bias transistor 120, 122. A first transistor 116 of the current steering mechanism 114 is coupled in the fourth current path 108, and is driven by feedback 124 from the third current path 106. A second transistor 118 of the current steering mechanism 114 is coupled in the fifth current path 110, and is driven by a reference voltage (VREF). The bias transistors 120, 122 are respectively coupled in the fourth and fifth current paths 108, 110, and mirror current to the first, second and third current paths 102-106 under control of the current steering mechanism 114 (with the bias transistor 120 in the fourth current path mirroring current to the first current path 102, and with the bias transistor 122 in the fifth current path mirroring current to the second and third current paths 104, 106).

[0014] The circuit 100 further comprises a second current mirror 126. The second current mirror 126 is driven by a bias current (IBIAS) and mirrors the bias current to each of the number of parallel current paths 102-110.

[0015] FIG. 2 illustrates a second exemplary circuit 200 for providing well-matched source and sink currents. The circuit 200 comprises a first current path 202 that provides well-matched source and sink currents (I1, I2) as outputs. The source current, I1, is provided through a first pair of series transistors 204, 206. A second current path 208 is coupled in parallel with

the first current path 202. The second current path 202 comprises a second pair of series transistors 210, 212, matched to the first pair of series transistors 204, 206.

[0016] A first current mirror 214 mirrors current to first corresponding transistors 204, 210 of the first and second pairs of series transistors; and a second current mirror 216 mirrors current to second corresponding transistors 206, 212 of the first and second pairs of series transistors.

[0017] A current steering mechanism 218 receives a feedback signal 220 from the second current path 208, as well as a reference signal (e.g., VREF), and steers current between the first and second current sources to match the feedback signal to the reference signal.

[0018] A third current mirror 222 mirrors a bias current (IBIAS) to the first and second current paths, the first current mirror 214, and the current steering mechanism 218.

[0019] FIG. 3 illustrates a third exemplary circuit 300 for providing well-matched source and sink currents. Of note, either of the circuits 100, 200 shown in FIGS. 1 or 2 may be implemented as shown in FIG. 3.

[0020] The circuit 300 comprises five parallel current paths 302-310. First and second of the parallel current paths 304, 306 may each comprise a pair of series transistors 312/314, 316/318 to source current from a voltage source (VDD). The transistors of each pair (e.g., pair 312/314) are coupled in series via their sources and drains and, preferably, all of the transistors of both pairs are similarly sized. By way of example, FIG. 3 shows that each series pair of transistors comprises p-channel field effect transistors (PFETs).

[0021] Transistor 320 is coupled in series with transistor 322 in a third current path 302. Transistors 320 and 322 are coupled with respect to each other to form an over-the-shoulder cascode current mirror (i.e., with the gate of transistor 320 coupled to node "pc" of current path 302). The gate of transistor 320 is further coupled to the gates of transistors 312, 316 in the first and second current paths 304, 306. In this manner, the transistors 312, 316, 320 form a first current mirror 324.

[0022] The first and second current paths 304, 306 may comprise matched pairs of transistors 312/316, 314/318, 334/336. That is, transistors 316, 318, 334 in the second current path 306 are matched to corresponding transistors 312, 314, 336 in the first current path 304. Preferably, each pair of transistors is laid out using common centroid layout techniques. The second current path 306 allows feedback to be obtained on output currents I1 and I2 with less of an impact on the output currents. Due to the matched structures of the first and second current paths 304, 306, feedback that could be derived from the first current path 304 should be substantially identical to feedback that is derived from the second current path 306.

[0023] Each of fourth and fifth current paths 308, 310 may comprise a transistor 344, 346 of a current steering mechanism 338, as well as a bias transistor 340, 342. The bias transistors may each take the form of a diode-connected PFET 340, 342 that is coupled gate-to-gate to with one or more corresponding PFETs 322, 314, 318 in the first, second and third current path 304, 306, 302. In one embodiment, the bias transistors 340, 342 are sized to about 25% of the driven transistors 314, 318, 322.

[0024] The current steering mechanism 338 may comprise an n-channel field effect transistor (NFET 344) that is coupled in the fourth current path 308 via its source and drain. The NFET 344 receives a feedback voltage (vf) at its gate. The feedback voltage (vf) is derived from the current path 306. The current steering mechanism 338 may also comprise a second NFET 346, coupled in the fifth current path 310 via its source and drain. The NFET 346 receives a reference voltage (VREF) at its gate. The drains of the steering mechanism's transistors 344, 346 are together at node "vbs".

[0025] A second current mirror 348 may comprise a plurality of NFETs 328, 330, 332, 334, 336 that couple each of the parallel current paths 302-320 to ground (GND) via their sources and drains. The gate of each NFET 328-336 is driven by the bias current (IBIAS), which is driven to the gates of the NFETs 328-336 by means of a diode-connected NFET 326. In this manner, the second current mirror 348 sinks current from each of the parallel current paths 302-310.

[0026] As configured in FIG. 3, the circuit 300 may be used to provide well-matched source and sink currents (I1 and I2) to any of a number of devices 350, including, for example, up/down current switches that serve as a charge pump to pump source and sink currents into a phase-locked loop in response to feedback received from the phase-locked loop. Preferably, the feedback path "vf" would include the same switching circuitry as device 350, but have control inputs hard-wired to their ON states.

[0027] FIG. 4 illustrates a method 400 for providing well-matched source and sink currents. By way of example, the method 400 may be executed using the circuits shown in any of FIGS. 1-3.

[0028] In accordance with the method 400, a bias current (IBIAS) is mirrored 402 to each of a number of parallel current paths of a circuit. Referring back to FIG. 3, one sees that this may be done using the transistors 326-336 of the second current mirror 348. The bias current is also mirrored 404 from a first of the parallel current paths to second and third of the parallel current paths. Referring back to FIG. 3 again, one sees that this may be done using the transistors 314, 316, 320 of the first current mirror 324.

[0029] The method 400 continues with the provision 406 of a reference voltage (e.g., VREF), and feedback from the circuit, to a current steering mechanism comprising fourth and fifth of the parallel current paths. Current is then steered 408 between the first, second and third current paths by means of the current steering mechanism. Depending on the value of VDD and other considerations, VREF can be adjusted to provide an appropriate bias for the circuit.

[0030] The method 400 concludes with the output 410 of well-matched source and sink currents from the second current path. By way of example, the source and sink currents (e.g., I1 & I2; FIG. 3) may be output to a phase-locked loop in response to feedback received from the phase-locked loop.

[0031] Embodiments of the circuits 100, 200, 300 and method 400 disclosed in FIGS. 1-4 provide various advantages over other circuits (e.g., circuits 500 & 600; FIGS. 5 & 6) and methods used to provide matched source and sink currents.

[0032] In FIG. 5, a diode-connected NFET 502 drives NFETS 504, 506 of a first current mirror, and a diode-connected PFET 508 drives a PFET 510

of a second current mirror, thereby providing source and sink currents (I1 and I2) to a device 512. Compared to the circuit 500 illustrated in FIG. 5, the circuits 100, 200, 300 and method 400 illustrated in FIGS. 1-4 can provide a higher output impedance and more precisely matched source and sink currents. The well-matched source and sink currents of circuits 100, 200, 300 are at least partly due to the feedback provided to the current steering mechanism of each circuit. Although feedback could be added to the circuit 500 illustrated in FIG. 5, this would require the overhead and complexity of an operational amplifier (op-amp). The output impedance of the circuit 500 could also be increased, but this is typically done using a cascode current source, and most cascode current sources require more power supply headroom than is generally available in today's integrated circuit (IC) processes.

[0033] The circuit 600 illustrated in FIG. 6 adds an additional current mirror leg 602, 604, 606 and over-the-shoulder cascode current mirror 602, 608 to the circuit 500 illustrated in FIG. 5. Compared to the circuit 500 illustrated in FIG. 5, the circuit 600 illustrated in FIG. 6 provides higher output impedance and more reasonable power supply headroom requirements. However, feedback is difficult to implement in the circuit 600 because the FETS 602 and 604 tend to correct for changes made to each other. The circuits 100, 200, 300 and method 400 illustrated in FIGS. 1-4, on the other hand, can provide all of the advantages of the circuit 600 illustrated in FIG. 6, but with the addition of an easily adjusted feedback mechanism. By incorporating feedback, the circuits 100, 200, 300 and method 400 illustrated in FIGS. 1-4 provides more precisely matched source and sink currents.

[0034] Another advantage provided by at least some embodiments of the circuits 100, 200, 300 and method 400 is the minimization of phase offsets.

[0035] While illustrative and presently preferred embodiments of the invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed, and that the appended claims are intended to be construed to include such variations, except as limited by the prior art.